

In the Claims

Please amend the claims as follows:

C1 1 1. (Currently Amended) A circuit for interfacing between a first  
2 component operating at a first clock rate and a second component  
3 operating at a second clock rate wherein said second clock rate is  
4 higher than said first clock rate, said circuit comprising:

5 a first buffer coupled to said first component, said first  
6 buffer receiving and storing data received from said first  
7 component at said first clock rate;

8 a second buffer coupled to said second component, said second  
9 buffer supplying data recalled therefrom to said second component  
10 at said second clock rate;

11 a copy/access controller connected to said first buffer, said  
12 second buffer, and said second component and operable to copy data  
13 from said first buffer to said second buffer when said first buffer  
14 is substantially full, and further operable to prompt said second  
15 component to access said second buffer when said data is copied  
16 from said first buffer.

1 2. (Original) The circuit as set forth in Claim 1, wherein both  
2 said first buffer and said second buffer are random-access  
3 memories.

1 3. (Original) The circuit as set forth in Claim 1, wherein both  
2 said first buffer and said second buffer are shift registers.  
3

4 4. (Original) The circuit as set forth in Claim 1, wherein said  
5 circuit is integrated onto a semiconductor die with one of said  
6 first component or said second component.

5 to 10 (Canceled)

C1 1 11. (Currently Amended) A method for interfacing between a first  
2 component operable at a first clock rate and a second component  
3 operable at a second clock rate wherein said second clock rate is  
4 higher than said first clock rate, comprising the steps of:  
5       transferring data from said first component to a first buffer  
6 operable at said first clock rate;  
7       copying data from said first buffer to a second buffer  
8 operable at said second clock rate when said first buffer is  
9 substantially full;  
10       prompting said second component to access said data in said  
11 second buffer at said second clock rate when said copying step is  
12 completed.

1 12. (Previously Presented) The method as set forth in Claim 11,  
2 wherein both said first buffer and said second buffer are shift-  
3 register structures.

1 13. (Previously Presented) The method as set forth in Claim 11,  
2 wherein both said first buffer and said second buffer are random  
3 access memories.

1 14. (Previously Presented) The method as set forth in Claim 11,  
2 wherein said first buffer and said second buffer are both  
3 integrated onto the same semiconductor die as one of said first  
4 component or said second component.